REMARKS:

Claims 1-55 were presented for examination and are pending in this application. In an Official Action dated April 13, 2005, claim 48 was objected to, and claims 1-55 were rejected. Applicants thank Examiner for examination of the claims pending in this application and address Examiner's comments below.

Applicants herein amend claims 1, 46, and 48. These changes are believed not to introduce new matter, and their entry is respectfully requested. The claims have been amended to expedite the prosecution of the application in a manner consistent with the Patent Office Business Goals, 65 Fed. Reg. 54603 (Sept. 8, 2000). In making these amendments, Applicants have not and do not narrow the scope of the protection to which Applicants consider the claimed invention to be entitled and do not concede that the subject matter of such claims was in fact disclosed or taught by the cited prior art. Rather, Applicants reserve the right to pursue such protection at a later point in time and merely seek to pursue protection for the subject matter presented in this submission.

Based on the above Amendment and the following Remarks, Applicants respectfully request that Examiner reconsider all outstanding objections and rejections, and withdraw them.

Response to Rejection Under 35 USC § 112, Paragraph 2

Claims 46-55 are rejected as not specifically pointing out and distinctly claiming the subject matter that the Applicant regards as the invention. Claim 46 is amended herein to provide proper antecedent basis to the first and second thread states. This amendment of the claim is made so as to more clearly define the invention, and not to narrow their scope of protection with respect to the prior art, or with respect to potentially infringing

devices/compositions/articles. Based on this amendment, applicants kindly request withdrawal of this rejection.

In addition, claim 48 is amended herein to correct a typographical error thereby overcoming Examiner's objection.

Response to Rejections Under 35 USC 102

Claims 1-3, 13-17, 19, 21-24, 29-32, and 42-46 are rejected under § 102(e) as allegedly anticipated by Joy. Applicants respectfully traverse this rejection.

Independent claims 1 and 46 have been amended to clarify the predetermined nature of the fixed schedule that provides a fixed timing component according to which threads are executed at a fixed time. Independent claim 1, as now amended, recites elements to indicate that the thread scheduling and selection is performed by the processor's hardware thread scheduler, which is

> configurable to allocate available processing time of the processor among at least the first and second threads by causing thread-switching at a fixed time according to a predetermined fixed schedule.

The scheduler is configurable to cause the processor to switch from one thread to another thread at a fixed time. This is greatly beneficial because it provides a predictable execution time for threads.

Joy does not teach or disclose "causing thread-switching at a fixed time" as recited in the claims. The Examiner stated that predetermined scheduling is anticipated by Joy because "before the system even begins running a program, it is known that the scheduler will schedule based on cache misses because that is how it was designed." However, the context switches in Joy "are made in response to interrupts, including hardware and software

interrupts, both internal and external, of a processor." Joy, col. 14, lines 62-63. Unlike the thread-switching recited in claim 1, the thread switching in Joy is not caused at a fixed time according to a predetermined fixed schedule; instead Joy's thread-switching is based on some external stimulus or signal, e.g., L1 data cache miss stall signal, instruction buffer empty signal, etc. (see Joy, col. 3, lines 28-56) that can happen randomly at any time; the time when the thread-switching events take place is not fixed. Thus, Joy does not teach causing thread-switching at a fixed time according to a predetermined fixed schedule.

Accordingly, for at least this reason, claim 1 is patentable over Joy. Applicants note that new claims 29-45 depend, directly or indirectly, from claim 1. Accordingly, they include the elements described above that are lacking in Joy. Hence, for at least the reasons set forth above, newly added claims 29-45 are also patentable over Joy. Applicants further note that claim 46 also recites elements that include the fixed time thread-switching according to a predetermined fixed schedule similar to that recited in claim 1. Hence, for at least the reason described above with respect to claim 1, claim 46 and its dependent claims 47-55 are also patentable over Joy.

Claim 17 is also distinguishable from Joy. Claim 17 recites that the processor "switches from said first thread state to said second thread state between consecutive instruction cycles." This allows the processor to perform "zero-time" context switching, which greatly increases the processor's speed.

As previously stated, Joy describes "fast, nanosecond range context switching." Joy, col. 14, line 48. However, the context switching described in Joy does not take place between consecutive instruction cycles. However fast it may be, the switching described in Joy produces an overhead of at least one processor cycle. See Joy, col. 16, lines 4-5. As

described in Joy, "[t]he thread switch logic supports fast thread switch with a very small delay, for example three cycles or less." Joy, col. 16, lines 61-62 (emphasis added).

Examiner's reliance in Fig. 2B as the basis for anticipation of this claimed feature is misguided. The Joy reference clearly states that FIGs. 2A, 2B, and 2C are "three highly schematic timing diagrams respectively illustrat[ing] execution flow 210 of a single-thread processor, execution flow 230 of a vertical multithreaded processor, ..." Inferring that because no idle time is shown between threads in this "highly schematic" figure (FIG. 2B) is indicative of switching in consecutive cycles is improper. Such inference is not supported by the detailed description of Joy.

One aspect of Joy's system includes "fast thread-switching". See, e.g., col. 3, lines 28-56. However, where timing of the thread switching process is described in detail, there is no mention of "consecutive cycles" or "zero-time" switching, as described and claimed by Applicants. The fastest thread switching described in Joy requires at least one overhead cycle (see, col. 16, lines 1-5). The Examiner incorrectly states that based on Joy's description, "if thread A is to execute in cycle X, and thread switch occurs, then thread B may be executed in cycle X+1." However Joy describes that there is at least one cycle of switching overhead. Thus, based on Joy's description if thread A is to execute in cycle X, a context switch takes place during overhead cycle X+1, and thread B may be executed at cycle X+2. Thus, Joy requires at least one overhead processor cycle. Accordingly Joy does not teach context switching between consecutive instruction cycles as recited in the processor of claim 17.

Therefore, for at least this reason, claim 17 and its dependent claims 2-16 and 18, are patentable over Joy. Similarly, claim 19 includes a "consecutive execution cycle" switching

element similar to that of claim 17. Therefore, for at least the reasons set forth above, claim 19, and its dependent claims 18-28 are patentable over Joy.

As shown above, at least claims 1-3, 13-17, 19, 21-24, 29-32, and 42-46 are patentable over the cited reference. Therefore, Applicants kindly request withdrawal of this rejection.

Response to Rejections Under 35 USC 103

In the 24th paragraph of the Office Action, Examiner rejects claims 4, 20, 33, and 47 under 35 USC § 103(a) as allegedly being unpatentable over Joy in view of U.S. Patent No. 6,567,839 to Borkenhagen et al. ("Borkenhagen"). Similarly, in the 26th paragraph of the Office Action, Examiner rejects claims 5-9, 18, 25-28, 34-38, and 48-55 under 35 USC § 103(a) as allegedly being unpatentable over Joy in view of U.S. Patent No. 6,085,215 to Ramakrishnan et al. ("Ramakrishnan"). And in the 36th paragraph of the Office Action, Examiner rejects claims 10-12, and 39-41 under 35 USC § 103(a) as allegedly being unpatentable over Joy in view of Ramakrishnan and further in view of U.S. Patent No. 6,026,503 to Gutgold et al. ("Gutgold"). This rejections are respectfully traversed.

The rejected claims, 4-9, 10-12, 18, 20, 25-28, 33-42, and 47-55 are dependent, directly or indirectly on claims 1, 17, 19, and 46. These independent claims recite elements, such as fixed time switching and consecutive-cycle context switching, that as discussed above, are lacking in the Joy reference. Accordingly, the Joy reference does not anticipate these independent claims, or their dependent claims 4-9, 10-12, 18, 20, 25-28, 33-42, and 47-55.

The Examiner cited Borkenhagen to make up for the deficiency of a "state selection register" in Joy. However, the combined Joy- Borkenhagen reference still fails to teach or

suggest the fixed time or consecutive-cycle switching recited in the claims. In fact, the system of Borkenhagen incurs the conventional "latency and performance penalties associated with switching threads." (Borkenhagen, col. 15:37-38).

> In the multithreaded processor in the preferred embodiment described herein, this latency includes the time required to complete execution of the current thread to a point where it can be interrupted and correctly restarted when it is next invoked, *the time required to switch the thread-specific hardware facilities from the current thread's state to the new thread's state*, and the time required to restart the new thread and begin its execution.

Borkenhagen, col. 15:38-46 (emphasis added).

Likewise, Ramakrishnan is cited to make up for Joy's lack of "thread identifier for identifying at least one hard-real-time (HRT) thread and at least one non-real-time thread" limitation. However, the Joy-Ramakrishnan combined reference still fails to teach or suggest the fixed time or consecutive-cycle context switching recited in the claims. Ramakrishnan simply describes a software scheduler that uses a round robin approach to thread scheduling using conventional context switching. See Ramakrishnan, col. 9, lines 9-10. The switching in Ramakrishnan, like in Borkenhagen, is conventional context switching that involves "an associated overhead in invoking the new thread." Ramakrishnan, col. 12, lines 61-62, see also, col. 13, lines 6-7 ("avoid time consuming context switching").

Finally, Gutgold is relied upon to provide the different access speed memory devices recited in claims 10-12 that are not explicitly described in Joy or Ramakrishnan. However, the combined Joy-Ramakrishnan-Gutgold reference still fails to teach or suggest the fixed time or consecutive-cycle context switching recited in the claims. Gutgold does not describe any context switching. Aside from the fact that Gutgold describes a microprocessor

controlled system and associated microprocessor system components, Applicants see no other relation to Applicants' invention.

Accordingly, for at least the reasons set forth above, claims 4-9, 10-12, 18, 20, 25-28, 33-42, and 47-55 are patentable over the cited combined references. Thus, Applicants kindly request withdrawal of these rejections.

Conclusion

Applicants respectfully submit that claims 1 through 55 as presented herein are patentably distinguishable over the cited references. Accordingly, Applicants respectfully request allowance of all pending claims.

In addition, Applicants respectfully invite Examiner to contact Applicants' representative at the number provided below if Examiner believes it will help expedite furtherance of this application.

Respectfully Submitted,
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Date: July 13, 2005 By: _____

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